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PTO/SB/05 (12/97)
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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No. 503.35443VX1 Total Pages 10

First Named Inventor or Application Identifier

NAGAI, et al.

Express Mail Label No.

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. Fee: \$846.00

6. Microfiche Computer Program (Appendix)

Please charge any shortages in the fees or credit any overpayments thereof to the deposit account of Antonelli, Terry, Stout & Kraus, Deposit Account No. 01-2135.

7. Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)

- a. Computer Readable Copy
- b. Paper Copy (identical to computer copy)
- c. Statement verifying identity of above copies

2. Specification Total Pages 45

ACCOMPANYING APPLICATION PARTS

8. Assignment Papers (cover sheet & document(s))

3. Drawing(s) (35 USC 113) Total Sheets 5

9. 37 CFR 3.73(b) Statement (when there is an assignee) Power of Attorney

4. Oath or Declaration Total Pages 3

10. English Translation Document (if applicable)

a. Newly executed (original or copy)

11. Information Disclosure Statement (IDS)/PTO-1449 Copies of IDS Citations

b. Copy from a prior application (37 CFR 1.63(d)) (for continuation/divisional with Box 17 completed)

12. Preliminary Amendment

i. DELETION OF INVENTOR(S)

13. Signed statement attached deleting (Should be specifically itemized)

Signed statement attached deleting
inventor(s) named in the prior application,
see 37 CFR 1.63(d)(2) and 1.33(b).

14. Small Entity Statement filed in prior application,
Statement(s) Status still proper and desired

5. Incorporation By Reference (useable if Box 4b is checked)

15. Certified Copy of Priority Document(s)
(if foreign priority is claimed)

The entire disclosure of the prior application, from which a
copy of the oath or declaration is supplied under Box 4b,
is considered as being part of the disclosure of the
accompanying application and is hereby incorporated by
reference therein.

16. Other: Claim for Priority

17. If a CONTINUING APPLICATION, check appropriate box and supply the requisite information:

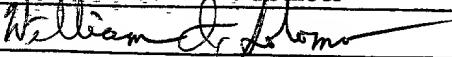
Continuation Divisional Continuation-In-Part (CIP)

of prior application No. 08,857,674

18. CORRESPONDENCE ADDRESS

Customer Number or Bar Code Label 020457
(Insert Customer No. or Attach bar code label here)

11. SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

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Title of the Invention

CIRCUIT TAPE HAVING ADHESIVE FILM, SEMICONDUCTOR
DEVICE, AND A METHOD FOR MANUFACTURING THE SAME

5 This application is a Divisional application of
application Serial No. 08/857,674, filed May 16, 1997.

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Background of the Invention

The present invention relates to a circuit tape, a semiconductor device, and a method of manufacturing the same, which are superior in electrical characteristics, mounting reliability, and assembling easiness, and are responsive to the requirements for high density mounting, multipins mounting, and fast transmittance.

20 Currently, in the continuing effort to improve electronic devices to provide high performance, the demand for high integration and high density mounting of semiconductor elements has become strong. Therefore, semiconductor elements have been improved to achieve high integration and high performance, such as in LSI, VLSI, and ULSI devices, and there has been increase in the capacity, the number of pins, the speed, and power consumption thereof. In responding to such advances, the package structure of the semiconductor device for multipins has been changed from a structure, in which connecting terminals are provided at two sides of the semiconductor element, to an advanced structure, in which the connecting terminals are provided at all four sides of the semiconductor element. Furthermore, in order to respond to increasing the number of pins, a grid array structure has come to be used in

25

practice. The grid array structure is a structure of a semiconductor element, in which the connecting terminals are provided in a grid array over the entire mounting surface of the semiconductor element by using a multilayer carrier substrate. The grid array structure includes a ball grid array structure (BGA), which has a shortened connecting terminal length in order to make fast signal transmission possible. The ball type structure of the connecting terminal increases the width of its conductor; therefore, the ball structure is also effective in decreasing inductance. Currently, in order to respond to the requirement for fast signal transmission, organic materials having a relatively low dielectric constant have been investigated for use in the multilayer carrier substrate. However, the organic materials have generally a larger thermal expansion coefficient than the semiconductor element, and so thermal stress generated by the difference in thermal expansion becomes a problem from the point of view of connection reliability, and so on. Recently, a structure which does not use a carrier substrate has been proposed for the BGA package.

More particularly, a new semiconductor element package structure has been disclosed (US Patent 5,148,265), in which the connection reliability is improved by using an elastomer material having a low modulus of elasticity for reducing the thermal stress generated by the difference in thermal expansion between the semiconductor element and the mounting substrate. The proposed package structure uses a circuit

tape composed of a polyimide and the like, instead of a carrier substrate, for electrically connecting the semiconductor element and the mounting substrate. Therefore, the electrical connections between the semiconductor element and the circuit tape are effected by a wire bonding method or a bonding connection with leads, and the circuit tape and the mounting substrate are electrically connected by soldering ball terminals. As the elastomer material of the prior art, a silicone material is generally used since this is a material having a low modulus of elasticity and a superior heat resistance. As a general method for forming a stress buffer layer with a silicone material, the steps of printing an uncured liquid resin on the circuit tape using masks, and subsequently, curing the printed resin, are generally used. However, the above method has problems, such as a difficulty in maintaining the flatness of the buffer layer obtained by the printing, and the complexity of the printing process, which requires a long time for the printing, is disadvantageous.

Accordingly, the above method is not suitable for a mass-production process, and so the problems which undesirably affect the assembling yield and reliability of mounting caused by the difficulty in maintaining the flatness of the buffer layer are yet to be solved.

Summary of the Invention

One of the objects of the present invention is to provide a method of obtaining a stress buffer layer which is superior in flatness by using a film material as the

elastomer material for reducing the thermal stress in the semiconductor devices, thereby obtaining semiconductor devices which are superior in mass productivity.

In order to realize the above object, the present invention provides the following measures.

The measures can be achieved by providing a semiconductor device comprising a circuit tape having a pattern layer connected electrically to a semiconductor element, an external terminal provided on the circuit tape for electrically connecting the circuit tape to a mounting substrate, and film material for causing the circuit tape to adhere to the semiconductor element while maintaining an insulation condition between the circuit tape and the semiconductor element, wherein the film material for effecting the adhering has a physical property such that the modulus of elasticity of the film material in the temperature range of a solder reflow condition for mounting (200 - 250°C) is at least 1 MPa.

The above film material for effecting the adhering is passed through a process for forming an external terminal, such as a solder ball and the like, for connecting the mounting substrate and the circuit tape, or a solder reflow process for mounting the semiconductor element of the present invention onto a mounting substrate in the manufacturing process of the semiconductor devices. The reflow temperature is generally a high temperature in the range of 200 - 250°C. Therefore, if the semiconductor device contains moisture, the moisture evaporates during the

heat treatment, and the film material swells due to the vapor pressure of the moisture. When the swelling exceeds a threshold value, a foaming phenomenon is generated, and defects, such as void formation, delamination, and the like, are generated. Therefore, the film material to be used is required to have as low a moisture absorption rate as possible and a high modulus of elasticity in the range of the reflow temperature. In accordance with the present invention, various film materials have been studied, and it was found that the adhesive materials having a modulus of elasticity in the temperature range of a reflow process of at least 1 MPa had superior reflow characteristics. Several examples of the temperature dependence of the modulus of elasticity of the material are shown in Fig. 1.

Furthermore, it was found that when materials, of which the modulus of elasticity in the temperature range of the mounting reflow condition was maintained at least at 1 MPa, were used, a preferable result in the anti-reflow characteristics could be obtained. The amount of swelling depends on the ratio of the vapor pressure and the modulus of elasticity, and the higher the modulus of elasticity is, the less will be the amount of swelling. The foaming phenomenon is generated when the amount of swelling exceeds the break elongation, one of the mechanical properties of the material. Furthermore, the modulus of elasticity correlates with the mechanical strength of the adhesive film material, and generally, the higher the modulus of elasticity is, the greater will be the tendency to increase

the break stress and break elongation. Therefore, by using a material having a high modulus of elasticity in the range of the reflow temperature, the reflow characteristics can be improved as to both the swelling amount and the mechanical characteristics. In the above case, the adhesive film material may be either a thermosetting resin or a thermoplastic resin.

The adhesive layer is sometimes composed of either sticky adhesive agents or sticky-cohesive adhesive agents, in addition to the adhesive agents made of the above material. In order to maintain the modulus of elasticity at least at 1 MPa in the temperature range of the reflow process, the thermoplastic resin preferably has a glass transition temperature, i.e. a changing point of modulus of elasticity, which is higher than the temperature range (200 - 250°C) of the reflow process. The thermosetting resin is required to have a chemical or physical crosslinking structure to a certain degree at a temperature in the rubber region, which is higher than the glass transition temperature. That is, the modulus of elasticity in the rubber region is generally proportional to the crosslinking density, and the crosslinking density must be increased in order to increase the modulus of elasticity. The film material is desirably composed of a resin having a low modulus of elasticity which is at the utmost 4000 MPa at room temperature, in order to operate as a stress buffer layer.

As one of characteristics of a film material, the

coefficient of moisture absorption at 85°C/85% RH for 168 hours is desirably, at the utmost, 3% in view of the reflow characteristics. As the film material, materials having a low modulus of elasticity, except for a silicone material, can be used. The structure of the film material is not restricted to a homogeneous structure composed of an adhesive agent component, but also, for instance, a three layer structure having adhesive layers at both surfaces of a supporter, respectively, or a structure in which the adhesive agent is impregnated into a porous supporter, can be used. As shapes of the film, various shapes manufactured by stamping, a mesh-like shape, and the like can be used. The mesh-like shape is effective in improving the anti-reflow property at the moisture absorbing time, because the adhesion area can be decreased.

In the case of a multilayer structure represented by a three layer structure, the supporter and the adhesive layer can be composed of a combination of at least two kinds of the above adhesive agents, the sticky adhesive agents, the sticky-cohesive adhesive agents, and the like. The adhesive layer is located at each of both of the surfaces of the supporter, and each adhesive layer can be formed of a different kind of material from the other. For instance, a combination is usable in which a thermosetting resin having a high fluidity is used in order to flatten or eliminate the unevenness of the pattern layer of the circuit tape side, and a thermoplastic resin, which can be adhered in a short time at a high temperature, is used at the opposite flat

portion for adhering to the semiconductor element.

A set of schematic illustrations indicating a flow of a general fabrication process for the manufacture of semiconductor devices, according to the present invention, is shown in Fig. 2.

The process can be divided into three representative sections. The first one, including STEPS 1-5 (Fig. 2a), is a method for fabricating a semiconductor element comprising (1) the step 1 of applying an adhesive film to the tape having a pattern layer, (2) the step 2 of adhering the tape having a pattern layer to the semiconductor element by means of the adhesive film while maintaining an insulating condition therebetween, (3) the step 3 of electrically connecting the pattern layer formed on the tape and the pad on the semiconductor element, (4) the step 4 of sealing the electrically connected portion with an insulating agent, and (5) the step 5 of forming an external terminal on the tape for connection to the mounting substrate.

The above method is effective in improving the processability, because the circuit tape and the film material can be handled in the manner of a reel to reel process, as will be explained later.

The second one, including STEPS 6-10, (FIG. 2b), is a method for fabricating a semiconductor element comprising (1) the step 6 of applying an adhesive film to the semiconductor element, (2) the step 7 of adhering the tape having a pattern layer to the semiconductor element by means of the adhesive film while maintaining an insulating

condition therebetween, (3) the step 8 of electrically connecting the pattern layer formed on the tape and the pad on the semiconductor element, (4) the step 9 of sealing the electrically connected portion with an insulating agent, and (5) the step 10 of forming an external terminal on the tape for connection to the mounting substrate.

The above method is effective in improving the production yield of the semiconductor element itself. In accordance with the method, the stress buffer layer can be formed on the semiconductor element at the wafer stage condition.

The third one, including STEPS 11-14, (Fig. 2c), is a method of fabricating a semiconductor element comprising (1) the step 11 of setting the tape having the pattern layer in registration and adhering the tape to the semiconductor element using the adhesive film simultaneously with maintaining an insulating condition therebetween, (2) the step 12 of electrically connecting the pattern layer formed on the tape and the pad on the semiconductor element, (3) the step 13 of sealing the electrically connected portion with an insulating agent, and (4) the step 14 of forming an external terminal on the tape for connection to the mounting substrate.

The above method is effective in shortening the manufacturing time, because the number of steps in the process can be decreased.

These methods essentially comprise the following steps. The adhesive film material of the present invention is

provided between the tape material having the pattern layer and the semiconductor element by adopting a certain method, and the tape material and the semiconductor element are bonded together simultaneously or sequentially under conditions of designated temperature, pressure, and time.

Subsequently, the pattern layer on the tape is electrically connected to the connecting pad of the semiconductor element. As examples of a connecting method using a connecting lead previously formed on the circuit tape as a circuit for connection with the semiconductor element, any one of a single point bonding method, a gang bonding method, and the like can be used.

As another example of a method for connection, a method in which the pattern layer and the semiconductor element are connected with wire bonding can be adopted.

Then, the connecting portion is encapsulated with an insulating material, and finally the external terminals, which are electrically connected with the mounting substrate, are formed on the circuit tape. As an external terminal, a solder ball is generally used, and most of the solder ball is formed by plating. Metals which may be used for the plating are gold, nickel, copper, solder, and the like.

In order to improve the mass productivity in the manufacturing process, the process for integrating the adhesive film material with the circuit tape previously as shown in Fig. 2a is important.

As a general method for the above process, a method

comprising the steps of transferring the tape, whereon the pattern is formed, by a long reel apparatus, stamping out the adhesive film into a designated shape, and adhering the adhesive film of the designated shape onto the circuit tape, as shown in Fig. 3, is effective for mass production. When the adhesive film is made of a thermosetting resin, the adhesive film can be made to adhere to the circuit tape while in an uncured A stage or a half-cured B stage. The resin is then further cured to a condition of a final-cured C stage during the step of adhering the obtained circuit tape, to which the adhesive film is attached, to the semiconductor element. Otherwise, if the adhesive agent reaches the condition of the final cured C stage during the time that the adhesive film is adhered to the circuit tape, sometimes, an adhesive layer is newly formed on the cured film portion.

As a method for forming the adhesive layer, an application method, a film adhering method, and the like are generally used. The adhesive component is desirably not sticky at room temperature, but if sticky, a mold releasing paper and the like is used.

Fig. 4 shows an example of the composition of a circuit tape to which an adhesive film is attached. The circuit tape can be adhered to the semiconductor element. If a thermosetting resin is used for the adhesive layer at the circuit tape side and a thermoplastic resin is used for the adhesive layer at the side adhered to the semiconductor, the circuit tape having the adhesive ability shown in Fig. 4 can

be provided readily.

When the adhesive layer is composed of a thermoplastic, sticky, or cohesive material, the conditions for the two steps to adhere to the circuit tape and to the semiconductor element can be set as quite the same with respect to each other. As opposed to the case of a thermosetting resin, the curing reaction does not need to be controlled at the intermediate stages, and so a manufacturing process superior in workability can be provided.

When the adhesive layer is composed of a sticky or cohesive material, the material is advantageous from the point of view of avoiding warpage of the semiconductor element, because the material can be adhered at room temperature. When the adhesive film is initially combined with the circuit tape, the semiconductor element is easily registered at the time of adhering to the circuit tape. Accordingly, the jigs of the adhering apparatus can be simplified, and the method becomes advantageous for mass production.

With the semiconductor device relating to the present invention, the unevenness of the pattern circuit on the circuit tape is sometimes eliminated by filling spaces with the adhesive layer of the film. In this case, the suitability of the adhesive layer for the filling can be confirmed at the step of combining the circuit tape and the semiconductor element. Therefore, an unsuitable adhesive layer can be eliminated before joining the circuit tape to the semiconductor element, a loss of the semiconductor can

be avoided, and an advantageous increase in the production yield can be attained.

Typical examples of a thermosetting resin and a thermoplastic resin for the adhesive component of the film materials are as follows: epoxy resin, polyimide resin, polyamide resin, cyanate resin, isocyanate resin, fluorine-containing resin, silicon-containing resin, urethane resin, acrylate resin, styrene resin, maleimide resin, phenolic resin, unsaturated polyester resin, diallyl phthalate resin, cyanamide resin, polybutadiene resin, polyamideimide resin, polyether resin, polysulfone resin, polyester resin, polyolefine resin, polystyrene resin, polyvinyl chloride, transpolyisoprene resin, polyacetal resin, polycarbonate resin, polyphenylene ether resin, polyphenylene sulfide resin, polyacrylate resin, polyether imide resin, polyether sulfone resin, polyether ketone resin, liquid crystalline polyester resin, polyallylether nitrile resin, polybenzimidazole resin, various kinds of polymer blend, and polymer alloys, and the like.

The above examples of a thermosetting resin and a thermoplastic resin involve materials having an adhesiveness resulting from melting or softening of the material by heating. On the contrary, the sticky or cohesive materials are materials having an adhesiveness produced by pressurizing.

Typical examples of the sticky and cohesive materials are as follows: various rubber groups, such as the silicone group, the butadiene group and the isoprene group, acrylate

groups, polyvinyl ether groups, and the like. The cohesive material includes a room temperature curing type, a type cured by heat, ultraviolet ray irradiation, electron beam irradiation, and the like, a type cured by concurrent use of an accelerator, and the like. The room temperature curing type includes a moisture-reactive type which reacts in the presence of moisture in the atmosphere, a photo-reactive type which contains a photo-initiator, and an anti-oxygen material which contains peroxide, and the like. The thermosetting resin generally includes a crosslinking agent, such as thiurum groups, phenol groups, isocyanate groups, and the like, and adhesive components are crosslinked three-dimensionally to form the adhesive layer at a designated temperature.

The material of the type cured by ultraviolet ray irradiation, or electron beam irradiation, contains various photo-initiators. The material of the type cured by concurrent use of an accelerator includes a solution containing a reaction accelerator and a crosslinking agent, which are applied onto the surface of the sticky layer, wherein the adhesive layer is finally formed by mixing the above two agents with a contact pressure and reacting the two agents sequentially. For the cohesive agent of the present invention, a thermosetting resin is relatively preferable. Using a thermosetting resin, a semiconductor device, which is superior in mass productivity and reliability, can be provided by the method comprising the steps of registering the circuit tape and the semiconductor

element at room temperature, bringing the wiring tape and the semiconductor element into contact to form a set, and elevating the temperature of a plurality of such sets to a designated degree simultaneously in a container, such as a constant temperature bath, for producing a curing reaction to ensure the adhesive strength.

The modulus of elasticity of the adhesive film material is preferably high at a high temperature region in view of the reflow characteristics, but as low as possible at room temperature. In this regard, the semiconductor element and the mounting substrate generally have different thermal expansion coefficients from each other, and a thermal stress is generated, when the mounting is performed, at the external terminal, which is composed of a solder ball and the like. Then, the reliability of the connection becomes remarkably important.

If the modulus of elasticity of the adhesive film existing between the semiconductor element and the mounting substrate is low, the region of the adhesive layer becomes a stress buffer layer, and this is advantageous from the point of view of the connection reliability. The modulus of elasticity at room temperature is desirably, at the utmost, 4000 MPa. More preferably, the modulus of elasticity in the entire range of the heat cycling test (-55°C - 150°C) is, at the utmost, 2000 MPa. As a material which has a high modulus of elasticity at a high temperature and a relatively low elastic modulus in a range of a low temperature including room temperature, sometimes silicone group

materials are used. A film material comprising a silicone group material is one of the significantly important materials of the present invention.

However, film materials, other than the silicone group material having the above characteristics, are advantageous in comparison with the silicone group material. That is, because of the weak cohesive energy of silicon, cyclic low molecular weight silicone group compounds are gradually decomposed thermally during a long heat treatment, such as during storing at a high temperature (for instance, at least 150°C), and this sometimes becomes a cause of contamination to the environment.

The composition of the film material of the present invention is not only a homogeneous structure composed of the adhesive agent components, but also may be a three layer structure, such as a supporter having adhesive agent layers at both surfaces for instance, and a structure in which the adhesive agent is impregnated into a porous supporter. As the supporter of the film material, films or a porous material made of polyimide, epoxy, polyethylene terephthalate, cellulose, acetate, fluorine-containing polymer, and the like can be used.

As the shape of the film, the various shapes obtainable by stamping out, a mesh-like shape, and the like can be used. The mesh-like shape is effective in improving the anti-reflow properly at the moisture absorbing time, because the adhesion area can be decreased. The three layer structure can be controlled to an arbitrary thickness and as

to the kind of the adhesive layer provided at both the surfaces of the supporter, and the fluidity of the adhesive layer at the time of adhesion can be readily controlled. Furthermore, the presence of an insulating layer is ensured by the supporter located between the adhesive layers.

The value of vapor pressure of the adhesive material by moisture absorption at the time of reflow can be maintained at a low value by using the material, of which the film material has a coefficient of moisture absorption at 85°C/85% RH of, at the utmost, 3%, and so preferable reflow characteristics can be obtained.

The tape having a pattern layer is generally composed of a flexible circuit substrate. That is, a polyimide group material serving as the insulating layer, an epoxy group material, a polyimide group material, a phenolic group material, a polyamide group material, and the like are used as the adhesive layer with the conductor. Generally, copper is used as the conductor. As the wiring circuit, the copper is sometimes coated with nickel, gold plating, and the like. As the flexible circuit substrate, a material, which does not use the adhesive layer with the conductor, but uses a copper layer formed directly onto the polyimide insulating layer, is sometimes used.

The tape having a pattern layer is sometimes composed of a multilayer wiring structure. In this case, a voltage layer, a ground layer, and so on in addition to the signal layer can be formed in the circuit tape, and so a semiconductor device which is superior in electric

characteristics can be provided.

Two typical arrangements of the pad terminal on the semiconductor element for electrically connecting the tape material having the pattern layer with the semiconductor element are as follows.

The one is a peripheral pad arrangement as shown in Fig. 5. In this case, there are different types of structure for the arrangement of the external terminal of the semiconductor device, as shown in Figs. 6-1, 6-2, 6-3. That is, the case wherein the external terminals are located under the semiconductor element (Fan In type, Fig. 6 1), the case wherein the external terminals are located outside the semiconductor element (Fan Out type, Fig. 6-2), and the case wherein the external terminals are located at both under and outside the semiconductor element (Fan In/Out type, Fig. 6-3) can be used.

Another example of the pad arrangement is the central arrangement shown in Fig. 7. In this case, the semiconductor device is composed of the structure shown in Fig. 8.

In accordance with the present invention, the semiconductor element is a device wherein IC, LSI, and the like, such as memories, logic devices, gate arrays, customs, power transistors, and the like, are formed on a wafer comprising semiconductor materials such as Si, GaAs, and the like, and the device has terminals for connecting to a lead, bump, and the like.

In accordance with the present invention, the

semiconductor device comprising a tape having a pattern layer is used as an interconnection between the semiconductor element and the mounting substrate, which is superior in anti-reflow characteristics and connection reliability, may be provided by using a film material having a modulus of elasticity of at least 1 MPa in the reflow temperature region (200 - 250°C), which is a high temperature region, as the adhesive material while maintaining the insulation between the circuit tape and the semiconductor element. By using such a film material, a manufacturing method which is superior in mass productivity to the conventional printing methods can be provided.

Brief Description of the Drawings

These and other objects, features and advantages of the present invention will be understood more clearly from the following detailed description with reference to the accompanying drawings, wherein:

Fig. 1 is a graph indicating temperature dependency of the modulus of elasticity of materials;

Figs. 2a, 2b, and 2c are schematic illustrations indicating the manufacturing process of the semiconductor device of the present invention, wherein Fig. 2a shows a method wherein the film is adhered previously to the circuit tape, Fig. 2b shows a method wherein the film is adhered previously to the semiconductor element, and Fig. 2c shows a method wherein the circuit tape and the semiconductor element are adhered together simultaneously via the film;

Fig. 3 is a schematic diagram indicating the continuous

process for adhering the film using a long reel;

Fig. 4 is a schematic diagram showing a cross section indicating the composition of a circuit tape having a film with an adhesive agent layer;

5 Fig. 5 is a schematic diagram of a semiconductor element having peripheral pads;

Figs. 6-1, 6-2, 6-3 are schematic cross sections showing the structure of semiconductor devices using the semiconductor elements having the peripheral pads;

10 Fig. 7 is a schematic diagram showing a semiconductor element having pads located at the center of the element; and

15 Fig. 8 is a schematic cross section showing the structure of a semiconductor device using a semiconductor element having pads located at the center of the element.

Description of the Preferred Embodiments

(Embodiment 1)

An epoxy group adhesive film (made by Hitachi Chemical Co., Ltd., AS 3000, 50 μm thick) was registered, placed, and 20 adhered between a semiconductor element and circuit tape at 170°C for one minute with a pressure of 50 kgf/cm², and was then post-cured at 180°C for 60 minutes in a constant temperature bath. Subsequently, connecting leads on the circuit tape were electrically connected to pads of the 25 semiconductor element by single point bonding. The connecting portion was encapsulated with an epoxy encapsulant (made by Hitachi Chemical Co., Ltd., RC021C). Finally, the semiconductor device shown in Fig. 6-1 was

obtained by fixing the solder balls, which were connecting terminals with the mounting substrate, onto the circuit tape.

After absorbing moisture in a constant temperature bath at 85°C/85% RH for 168 hours, the obtained semiconductor device was set in an infrared reflow apparatus with a maximum temperature of 245°C, and it was confirmed whether the semiconductor device exhibited defects, such as delamination and voids by foaming the adhesive layer.

Furthermore, the connection reliability between the lead of the semiconductor device and the solder bump was confirmed. In this case, a woven glass-epoxy copper clad laminate FR-4 (made by Hitachi Chemical Co., Ltd., MCI-E-67) was used as the mounting substrate. The reliability was evaluated by performing a thermal cycling test (-55°C - 150°C, 1000 times).

(Embodiment 2)

A film material having a three layer structure was obtained by applying an adhesive agent (made by Hitachi Chemical Co. Ltd., DF335), composed of a die bonding film material, onto both surfaces of a polyimide film (made by Ube Kosan Co., Ltd., SGA, 50 µm thick) to a thickness of 50 µm. The obtained film material was registered and adhered to circuit tape at 170°C for five seconds with a pressure of 30 kgf/cm². Under the above conditions, the unadhered adhesive layer exhibited a sufficient adhesive force to adhere to the semiconductor element. The circuit tape attached with the film material was adhered to the

semiconductor element at 200°C for one minute with a
pressure of 30 kgf/cm², and was then post-cured at 200°C for
60 minutes in a constant temperature bath. Subsequently,
connecting leads on the circuit tape were electrically
5 connected to pads of the semiconductor element by gang
bonding. The connecting portion was encapsulated with an
epoxy encapsulant (made by Hitachi Chemical Co., Ltd.,
RC021C). Finally, the semiconductor device shown in Fig.
6-2 was obtained by fixing the solder balls, which served as
10 connecting terminals with the mounting substrate, onto the
circuit tape.

The reflow characteristics and connection reliability
of the lead and the solder bump of the obtained
semiconductor device were confirmed by the same method as
15 the embodiment 1.

16 (Embodiment 3)

A low elastic adhesive film composed of an epoxy resin
and acrylic rubber (made by Hitachi Chemical Co. Ltd., trial
product, 150 μm thick) was registered, placed, and adhered
20 between the semiconductor element and the circuit tape at
180°C for 30 seconds with a pressure of 100 kgf/cm², and was
then post-cured at 180°C for 60 minutes in a constant
temperature bath. Subsequently, connecting leads on the
circuit tape were electrically connected to pads of the
semiconductor element by wire bonding. The connecting
25 portion was encapsulated with a silicone encapsulant (made
by Toshiba Silicone Co., Ltd., TSJ 3150). Finally, the
semiconductor device shown in Fig. 6-3 was obtained by

fixing the solder balls, which served as connecting terminals with the mounting substrate, onto the circuit tape.

The reflow characteristics and connection reliability of the lead and the solder bump of the obtained semiconductor device were confirmed by the same method as the embodiment 1.

(Embodiment 4)

A film material having a three layer structure was obtained by adhering a low elastic adhesive film composed of epoxy resin and acrylic rubber (made by Hitachi Chemical Co. Ltd., trial product, 50 μm thick) to both surfaces of a woven glass-epoxy resin laminate (obtained by eliminating a copper cladding by etching from both surfaces of MCL-E-679 made by Hitachi Chemical Co., Ltd.). The film material was registered, placed, and adhered between the semiconductor element and the circuit tape at 200°C for 20 seconds with a pressure of 80 kgf/cm², and was then post-cured at 180°C for 60 minutes in a constant temperature bath. Subsequently, connecting leads on the circuit tape were electrically connected to pads of the semiconductor element by single point bonding. The connecting portion was encapsulated with a silicone encapsulant (made by Toshiba Silicone Co., Ltd., TSJ 3153). Finally, the semiconductor device shown in Fig. 8 was obtained by fixing the solder balls, which serve as connecting terminals with the mounting substrate, onto the circuit tape.

The reflow characteristics and connection reliability

of the lead and the solder bump of the obtained semiconductor device were confirmed by the same method as the embodiment 1.

(Embodiment 5)

5 A LOC (Lead on chip) Film (made by Hitachi Chemical Co. Ltd., HM122U, 100 μm thick) having a three layer structure was registered and adhered to the circuit tape at 300°C for 2 seconds with pressure of 150 kgf/cm². In the adhering process, the film was stamped out into a designated shape using the long scale apparatus shown in Fig. 3, and the stamped film was adhered to the circuit tape continuously. 10 Because the adhesive layer of the film was made of a thermoplastic resin, the unadhered portion of the adhesive layer still had a sufficient adhering force to the semiconductor element.

15 The circuit tape with the film material was adhered to the semiconductor element at 300°C for 10 minutes with a pressure of 100 kgf/cm². Subsequently, connecting leads on the circuit tape were electrically connected to pads of the semiconductor element by single point bonding. The 20 connecting portion was encapsulated with an epoxy encapsulant (made by Hokuriku Toryo Co., Ltd. Chip coat 8107). Finally, the semiconductor device shown in Fig. 6-1 was obtained by fixing the solder balls, which served as 25 connecting terminals with the mounting substrate, onto the circuit tape.

The reflow characteristics and connection reliability of the lead and the solder bump of the obtained

semiconductor device were confirmed by the same method as the embodiment 1.

(Embodiment 6)

A thermoplastic polyimide film (made by Mitsui Toatsu Chemicals, Inc., Regulus PI-UAY, 100 μm thick) was registered and adhered to the semiconductor element at 250°C for 2 seconds with a pressure of 30 kgf/cm². The film had a sufficient adhesive force to adhere to the circuit tape.

The semiconductor element with the film material was adhered to the circuit tape at 250°C for 10 minutes with a pressure of 20 kgf/cm². Subsequently, connecting leads on the circuit tape were electrically connected to pads of the semiconductor element by wire bonding. The connecting portion was encapsulated with an epoxy encapsulant (made by Hokuriku Toryo Co., Ltd. Chip coat 8107). Finally, the semiconductor device shown in Fig. 6-2 was obtained by fixing the solder balls, which served as connecting terminals with the mounting substrate, onto the circuit tape.

The reflow characteristics and connection reliability of the lead and the solder bump of the obtained semiconductor device were confirmed by the same method as the embodiment 1.

(Embodiment 7)

A film material composed of a three layer structure having two different kinds of adhesive layers was obtained by applying a fluorine-containing polyimide (a reactant of hexafluorobisphenol AF and bis(4-aminophenoxyphenyl)

hexafluoropropane, glass transition temperature 260°C) onto one surface of a polyimide film (made by Ube Kosan Co. Ltd., SGA, 50 μm thick) to a thickness of 50 μm , and a polyetheretherketone (a reactant of dihydroxy-naphthalene and difluorobenzophenone, glass transition temperature 154°C) onto the other surface of the polyimide film to a thickness of 50 μm .

The obtained film material was registered and adhered to the circuit tape using the adhesive layer having a lower glass transition temperature. The adhesion condition was at 200°C for one minute with a pressure of 30 kgf/cm². Because the adhesive layer of the film was composed of a thermoplastic resin, the adhesive layer had a sufficient adhering force to adhere to the semiconductor element. The circuit tape with the film material was adhered to the semiconductor element at 300°C for ten seconds with a pressure of 80 kgf/cm². Subsequently, connecting leads on the circuit tape were electrically connected to pads of the semiconductor element by gang bonding. The connecting portion was encapsulated with an epoxy encapsulant (made by Hokuriku Toryo Co. Ltd., Chip coat 8107). Finally, the semiconductor device shown in Fig. 6-3 was obtained by fixing the solder balls, which served as connecting terminals with the mounting substrate, onto the circuit tape.

The reflow characteristics and connection reliability of the lead and the solder bump of the obtained semiconductor device were confirmed by the same method as

the embodiment 1.

(Embodiment 8)

A silicone adhesive agent (made by Shinetsu Chemical Co. Ltd., KE1820) was applied onto one surface of a silicone film (made by Toray Dow Corning Silicone Co. Ltd., JCR6126, 5 150 μm thick, press-fabrication) to a thickness of 20 μm . Then, the silicone film was registered and adhered to the circuit tape. The adhesion condition was at 150°C for one minute with a pressure of 30 kgf/cm². Furthermore, in order 10 to adhere to the semiconductor element, the silicone adhesive agent (made by Shinetsu Chemical Co. Ltd., KE1820) was applied onto the other surface of the silicone film to a thickness of 20 μm , and the circuit tape attached with the film material was adhered to the semiconductor element. The adhesion condition was at 200°C for 30 seconds with a 15 pressure of 20 kgf/cm². Subsequently, connecting leads on the circuit tape were electrically connected to pads of the semiconductor element by gang bonding. The connecting portion was encapsulated with a silicone encapsulant (made by Toray Dow Corning Silicone Co. Ltd., DA 6501). Finally, 20 25 the semiconductor device shown in Fig. 8 was obtained by fixing the solder balls, which serve as connecting terminals with the mounting substrate, onto the circuit tape.

The reflow characteristics and connection reliability of the lead and the solder bump of the obtained semiconductor device were confirmed by the same method as the embodiment 1.

25 (Embodiment 9)

Porous polytetrafluoroethylene (made by Japan Gore-tex Inc., 190 μm thick), both surfaces of which were applied with BT resin (Bismaleimide-Triazine resin), was registered and adhered to the circuit tape. The adhesion condition was at 150°C for one minute with a pressure of 30 kgf/cm². Because the adhesive layer of the film was in a B stage condition (half-cured condition), the adhesive layer had a sufficient adhering force to adhere to semiconductor element. The adhesion of the circuit tape with the film material to the semiconductor element was conducted at 200°C for 2 minutes with a pressure of 70 kgf/cm². Subsequently, connecting leads on the circuit tape were electrically connected to pads of the semiconductor element by gang bonding. The connecting portion was encapsulated with an epoxy encapsulant (made by Hitachi Chemical Co., Ltd. RO21C). Finally, the semiconductor device shown in Fig. 6-1 was obtained by fixing the solder balls, which were connecting terminals with the mounting substrate, onto the circuit tape.

20 The reflow characteristics and connection reliability of the lead and the solder bump of the obtained semiconductor device were confirmed by the same method as the embodiment 1.

25 (Embodiment 10)

A sticky tape having a three layer structure (made by Teraoka Seisakusyo, Ltd., Tape No. 760, 145 μm thick, silicone adhesive agent was applied onto both surfaces of

Kapton film (commercial name by Du Pont)) was registered and adhered to the circuit tape at room temperature for 5 seconds with a pressure of 50 kgf/cm^2 . In the adhering process, the film was stamped out into a designated shape using the long scale apparatus shown in Fig. 3, and the stamped film was adhered to the circuit tape continuously. Because the adhesive layer of the film was made of a sticky resin, the unadhered portion of the adhesive layer still had a sufficient adhering force to adhere to the semiconductor element.

The circuit tape with the film material was adhered to the semiconductor element at room temperature for 10 seconds with a pressure of 5 kgf/cm^2 . Subsequently, connecting leads on the circuit tape were electrically connected to pads of the semiconductor element by single point bonding. The connecting portion was encapsulated with a silicone encapsulant (made by Toshiba Silicone Co. Ltd. TSJ 3150). Finally, the semiconductor device shown in Fig. 6-2 was obtained by fixing the solder balls, which serve as connecting terminals with the mounting substrate, onto the circuit tape.

The reflow characteristics and connection reliability of the lead and the solder bump of the obtained semiconductor device were confirmed by the same method as the embodiment 1.

(Embodiment 11)

A cohesive tape having a three layer structure ($150 \mu\text{m}$ thick, butadiene adhesive agent was applied onto both

surfaces of unwoven aramide cloth (100 μm thick)) was registered and adhered between semiconductor and circuit tape at room temperature for 5 seconds with a pressure of 50 kgf/cm². Under the above condition, some correction of the registration was possible, because the adhesive layer was still in a cohesive condition. Then, the adhesive layer of the film was cured at 180°C for 60 minutes in a constant temperature bath to form a connecting state having a three dimensional crosslinking structure, because the adhesive layer was made of a cohesive resin.

Subsequently, connecting leads on the circuit tape were electrically connected to pads of the semiconductor element by single point bonding. The connecting portion was encapsulated with a silicone encapsulant (made by Toshiba Silicone Co., Ltd. TSJ 3150). Finally, the semiconductor device shown in Fig. 6-3 was obtained by fixing the solder balls, which serve as connecting terminals with the mounting substrate, onto the circuit tape.

The reflow characteristics and connection reliability of the lead and the solder bump of the obtained semiconductor device were confirmed by the same method as the embodiment 1.

(Embodiment 12)

A polyamic acid was prepared by reacting an equivalent of benzophenone tetracarboxylic acid dianhydride (made by Wako Pure Chemicals) and bis(4(2-aminophenoxyphenyl)ether) (synthetic chemical) at 5°C in dimethylacetamide. Then, the reactant was heated at 250°C to obtain polyimide. The

obtained polyimide 100 g was mixed with 4,4'-glycidyl-3,3',
5,5'-tetramethylbiphenylether (made by Yuka Shell) 19.5 g,
phenol novolac (made by Meiya Kasei) 10.6 g, and
5 triphenylphosphate (made by Wako Pure Chemicals) 0.2 g as a
catalyst in dimethylacetamide to obtain a varnish containing
a non-volatile component of 20% by weight. A film 100 μm
thick was prepared with the obtained varnish.

The prepared film was registered and adhered to the
10 circuit tape. The adhesion condition was at 170°C for ten
seconds with a pressure of 30 kgf/cm². Under the above
conditions, the unadhered portion of the adhesive layer had
a sufficient adhering force to adhere with semiconductor
element. The adhesion of the circuit tape with the film
material to the semiconductor element was conducted at 200°C
15 for one minute with a pressure of 30 kgf/cm². Subsequently,
a post-curing was performed at 200°C for 60 minutes in a
constant temperature bath. Then, connecting leads on the
circuit tape were electrically connected to pads of the
semiconductor element by gang bonding. The connecting
20 portion was encapsulated with an epoxy encapsulant (made by
Hitachi Chemical Co., Ltd. RC021C). Finally, the
semiconductor device shown in Fig. 6-2 was obtained by
fixing the solder balls, which serve as connecting terminals
25 with the mounting substrate, onto the circuit tape.

The reflow characteristics and connection reliability
of the lead and the solder bump of the obtained
semiconductor device were confirmed by the same method as
the embodiment 1.

(Embodiment 13)

A film having a three layer structure was prepared by applying the varnish obtained in the embodiment 12 onto the one surface of polyimide film (made by Ube Kosan Co. Ltd., SGA, 50 μm thick) to a thickness of 20 μm (thermosetting resin component), and the fluorine-containing polyimide, i.e. the varnish prepared in the embodiment 7, (the reactant of hexafluorobisphenol AF and bis(4-aminophenoxyphenyl) hexafluoropropane, with a glass transition temperature of 260°C) was applied onto the other surface of the polyimide film to a thickness of 10 μm (thermoplastic resin component). The film was registered and adhered to the circuit tape at the surface where the thermosetting resin component was applied. The adhesion condition was at 170°C for 10 seconds with a pressure of 30 kgf/cm². Then, a post-curing was performed at 200°C for 60 minutes in a constant temperature bath. Subsequently, the semiconductor element was adhered to the surface where the thermoplastic resin component was applied. The adhesion condition was at 350°C for 2 seconds with a pressure of 80 kgf/cm². Then, connecting leads on the circuit tape were electrically connected to pads of the semiconductor element by gang bonding. The connecting portion was encapsulated with an epoxy encapsulant (made by Hokuriku Toryo chip coat 8107). Finally, the semiconductor device shown in Fig. 6-2 was obtained by fixing the solder balls, which serve as connecting terminals with the mounting substrate, onto the circuit tape.

The reflow characteristics and connection reliability of the lead and the solder bump of the obtained semiconductor device were confirmed by the same method as the embodiment 1.

5 (Comparative example 1)

An elastomer of 150 μm thickness was formed by registering silicone resin (made by Toray Dow Corning Silicone Co. Ltd., JCR 6126) with the circuit tape and printing using metal masks. After the formation, post-curing was performed at 150°C for 60 minutes in a constant temperature bath. Then, the flatness of the elastomer was determined using a laser film thickness measuring apparatus. A silicone adhesive agent (made by Sinetsu Chemical Co. Ltd., KE 1820) was applied onto the surface of the elastomer a thickness of 20 μm as an adhesive layer for causing the semiconductor element to adhere to the circuit tape having the elastomer, and the circuit tape was registered and adhered to the semiconductor element. The adhesion was carried out at 150°C for one minute with a pressure of 30 kgf/cm². Then, connecting leads on the circuit tape were electrically connected to pads of the semiconductor element by gang bonding. The connecting portion was encapsulated with a silicone encapsulant (made by Toshiba Silicone, TSJ 3150). Finally, the semiconductor device shown in Fig. 6-1 was obtained by fixing the solder balls, which serve as connecting terminals with the mounting substrate, onto the circuit tape.

The reflow characteristics and connection reliability

of the lead and the solder bump of the obtained semiconductor device were confirmed by the same method as the embodiment 1.

(Comparative example 2)

5 A film having a three layer structure was prepared by applying a thermoplastic resin (polyamide 12, m.p. 175°C) having a melting point equal to or lower than 200°C onto both surfaces of a polyimide film (made by Ube Kosan Co. Ltd., SGA, 50 μm thick) as adhesive layers (30 μm thick).

10 The film having the three layer structure was used to prepare a semiconductor device using the same method as the embodiment 1, and the reflow characteristics and connection reliability of the lead and the solder bump of the obtained semiconductor device were confirmed by the same method as the embodiment 1.

15 (Comparative example 3)

20 A film having a three layer structure was prepared by applying an epoxy resin (made by Hitachi Chemical Co., Ltd., RO21C) having a high modulus of elasticity at room temperature onto both surfaces of a polyimide film (made by Ube Kosan Co. Ltd., SGA) as adhesive layers (20 μm thick).

25 The film having the three layer structure was used to prepare a semiconductor device by the same method as the embodiment 1, and the reflow characteristics and connection reliability of the lead and the solder bump of the obtained semiconductor device were confirmed by the same method as the embodiment 1.

Table 1

	Elastic modulus (MPa)		Reflow test	Thermal cycling test(1000 cycles)	
	Adhesive film (25°C)	Adhesive layers (average of 200 ~ 250 °C)		Lead open failure (%)	Bump open failure (%)
Emb.* 1	788	4.3	No void	0	0
Emb. 2	5000	1.5	No void	0	0
Emb. 3	960	3.6	No void	0	0
Emb. 4	4190	3.6	No void	0	0
Emb. 5	3750	13	No void	0	0
Emb. 6	3500	100	No void	0	0
Emb. 7	3500	2000, 15	No void	0	0
Emb. 8	10	2.5	No void	0	0
Emb. 9	2000	100	No void	0	0
Emb. 10	20	2.5	No void	0	0
Emb. 11	30	3.5	No void	0	0
Emb. 12	850	8.5	No void	0	0
Emb. 13	3300	2000, 8.5	No void	0	0
Com.※1	10	2.5	No void	10	0
Com. 2	1400	~ 0	Void	5	0
Com. 3	11000	1100	No void	80	100

*: Embodiment, ※: Comparative example.

Flatness of the elastomer: High and low difference of comparative example 1 was 50 μm to thickness of 150 μm , and all other samples within 5 μm .

Reflow test condition: Pretreatment: 85°C/85% RH, 48 hours, Water absorption 240°C \times 3 times, Infrared oven.

10

In accordance with the present invention, a semiconductor device is provided, wherein tape material having a circuit layer and a semiconductor element are electrically connected, an external terminal for effecting electrical connection with the mounting substrate is provided on the circuit tape, and a film material is used as the material for bonding the circuit tape and the semiconductor element in an insulating manner, resulting in a semiconductor device which is superior in anti-reflow property due to the use of the film material for the adhesion, of which the modulus of elasticity in the reflow temperature range is at least 1 MPa. A manufacturing method is also provided which is superior in mass productivity by using a film material at a portion for buffering thermal stress generated by a difference in thermal expansion of the semiconductor element and the mounting substrate.

20

25

The film material is superior in flatness, and a high and low difference within 5 μm can be ensured for a thickness of 150 μm , and so a manufacturing method which is superior in workability can be provided. In accordance with the stress buffering effect of the film material, the connection reliability of both the lead portion which electrically connects the circuit tape and the semiconductor

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element, and the bump which electrically connects the semiconductor device and the mounting substrate can be satisfied simultaneously in a temperature cycling test.

WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:
 - a semiconductor element;
 - a circuit tape having a circuit layer;
 - external terminals for electrically connecting the circuit tape to a mounting substrate; and
 - an adhesive film for adhering said circuit tape to said semiconductor element such that the circuit tape is insulated from the semiconductor element, wherein
 - said circuit layer is electrically connected to a pad of said semiconductor element and to said external terminals, and
 - said adhesive film is porous.
2. A semiconductor device as claimed in claim 1, wherein said adhesive film includes a three-layer structure having a porous support layer and two adhesive layers which are respectively applied onto both sides of said porous support layer.
3. A semiconductor device as claimed in claim 1, wherein said adhesive film has a structure of an adhesive agent impregnated into a porous support layer.
4. A semiconductor device as claimed in claim 1, wherein said circuit layer of said circuit tape is

electrically connected to said pad of said semiconductor element by a wire bonding.

5. A semiconductor device as claimed in claim 1, wherein the porous adhesive film includes a material selected from the group consisting of polyimide, epoxy, polyethylene terephthalate, cellulose, acetate, and fluorine-containing polymer.

6. A semiconductor device as claimed in claim 1, wherein the porous adhesive film includes a porous polytetrafluoroethylene layer, both sides of which have had bismaleimide-triazine resin applied thereto.

7. A semiconductor device comprising:
a semiconductor element;
a circuit tape having a circuit layer on a dielectric film;
an adhesive film, positioned between said semiconductor element and said circuit tape, for operating as a stress relaxing layer for relaxing thermal stress; and
external terminals for electrically connecting the circuit tape to a mounting substrate, wherein
said adhesive film comprises a porous support,
a plane having pads of said semiconductor element is adhered to said circuit tape by said adhesive film such that the circuit tape is insulated from the semiconductor element, connecting leads on said circuit tape are

electrically connected to said pads on said semiconductor element, and

 said external terminals for connecting to said mounting substrate are formed on said circuit tape.

8. A semiconductor device as claimed in claim 7, wherein said adhesive film has a structure of an adhesive agent impregnated into a porous support layer.

9. A semiconductor device as claimed in claim 7, wherein said adhesive film includes a three-layer structure having a porous support layer and two adhesive layers which are respectively applied onto both sides of said porous support layer.

10. A semiconductor device as claimed in claim 7, wherein a portion of each of said pads of said semiconductor element connecting to said circuit layer of said circuit tape is sealed with an insulating material.

11. A semiconductor device as claimed in claim 10, wherein said insulating material is an epoxy material.

12. A semiconductor device comprising:
 a semiconductor element;
 a circuit tape having a circuit layer on a dielectric film;
 an adhesive film positioned between said

semiconductor element and said circuit tape for operating as a stress relaxing layer for relaxing thermal stress; and

external terminals for electrically connecting the circuit tape to a mounting substrate, wherein

pads are arranged at one of a middle and a periphery of said semiconductor element,

said adhesive film comprises a porous support,

said circuit layer is connected to a plane having said pads of said semiconductor element via said adhesive film such that said circuit layer is insulated from the semiconductor element,

connecting leads on said circuit tape are connected to said pads of said semiconductor element, and

external terminals for electrically connecting the circuit tape to a mounting substrate are formed on said circuit tape.

13. A semiconductor device as claimed in claim 12, wherein said external terminals for electrically connecting the circuit tape to said mounting substrate are formed at a bottom side of said semiconductor element.

14. A semiconductor device as claimed in claim 12, wherein said external terminals for electrically connecting the circuit tape to said mounting substrate are formed at an exterior side of said semiconductor element.

15. A semiconductor device as claimed in claim 12,

wherein said external terminals for electrically connecting the circuit tape to said mounting substrate are formed at a respective one of a bottom side and an exterior side of said semiconductor element.

16. A semiconductor device as claimed in claim 12, wherein a portion of each of said pads of said semiconductor element connecting to said circuit layer is sealed with an insulating material.

17. A semiconductor device comprising:

- a semiconductor element;
- a circuit tape having a circuit layer on a dielectric film;
- an adhesive film for connecting said semiconductor element to said circuit tape such that the circuit tape is insulated from the semiconductor element;
- external terminals for electrically connecting the circuit tape to a mounting substrate; and
- an outer frame covering planes of said semiconductor element except one plane, wherein
 - plural pads are provided at a periphery of said semiconductor element which is not covered with said outer frame, the plural pads being provided in a plane, said circuit tape is connected to the plane having said pads of the semiconductor element and to said outer frame at an outer side of the plane having said pads, by said adhesive film,

said adhesive film comprises a porous support,
 said circuit layer of said circuit tape is
electrically connected to said plural pads of said
semiconductor element,

 a portion of each of said pads of said semiconductor
element electrically connecting to said circuit layer is
sealed with an insulating material, and

 said plural external terminals for electrically
connecting the circuit tape to said mounting substrate are
formed on said circuit tape arranged at the outer frame.

18. A semiconductor device comprising:

- a semiconductor element;
- a circuit tape having a circuit layer on a dielectric film;
- an adhesive film for connecting said semiconductor element to said circuit tape such that the circuit tape is insulated from the semiconductor element;
- external terminals for electrically connecting the circuit tape to a mounting substrate; and
- an outer frame covering planes of said semiconductor element except one plane, wherein
 - plural pads are provided at a periphery of said semiconductor element which is not covered with said outer frame, the plural pads being provided in a plane, said circuit tape is connected to the plane having said pads of the semiconductor element and to said outer frame at an outer side of the plane having said pads, by said

adhesive film,

 said adhesive film comprises a porous support,

 said circuit layer of said circuit tape is
electrically connected to said plural pads of said
semiconductor element,

 a portion of each of said pads of said semiconductor
element electrically connecting to said circuit layer is
sealed with an insulating material, and

 said plural external terminals for electrically
connecting the circuit tape to said mounting substrate are
formed on said circuit tape arranged both at the outer frame
and at the semiconductor element.

ABSTRACT OF THE DISCLOSURE

A semiconductor device having a superior connection reliability is obtained by providing a buffer body for absorbing the difference of thermal expansion between the mounting substrate and the semiconductor element in a semiconductor package structure, even if an organic material is used for the mounting substrate. A film material is used as the body for buffering the thermal stress generated by the difference in thermal expansion between the mounting substrate and the semiconductor element. The film material has modulus of elasticity of at least 1 MPa in the reflow temperature range (200 - 250°C).

FIG. 1

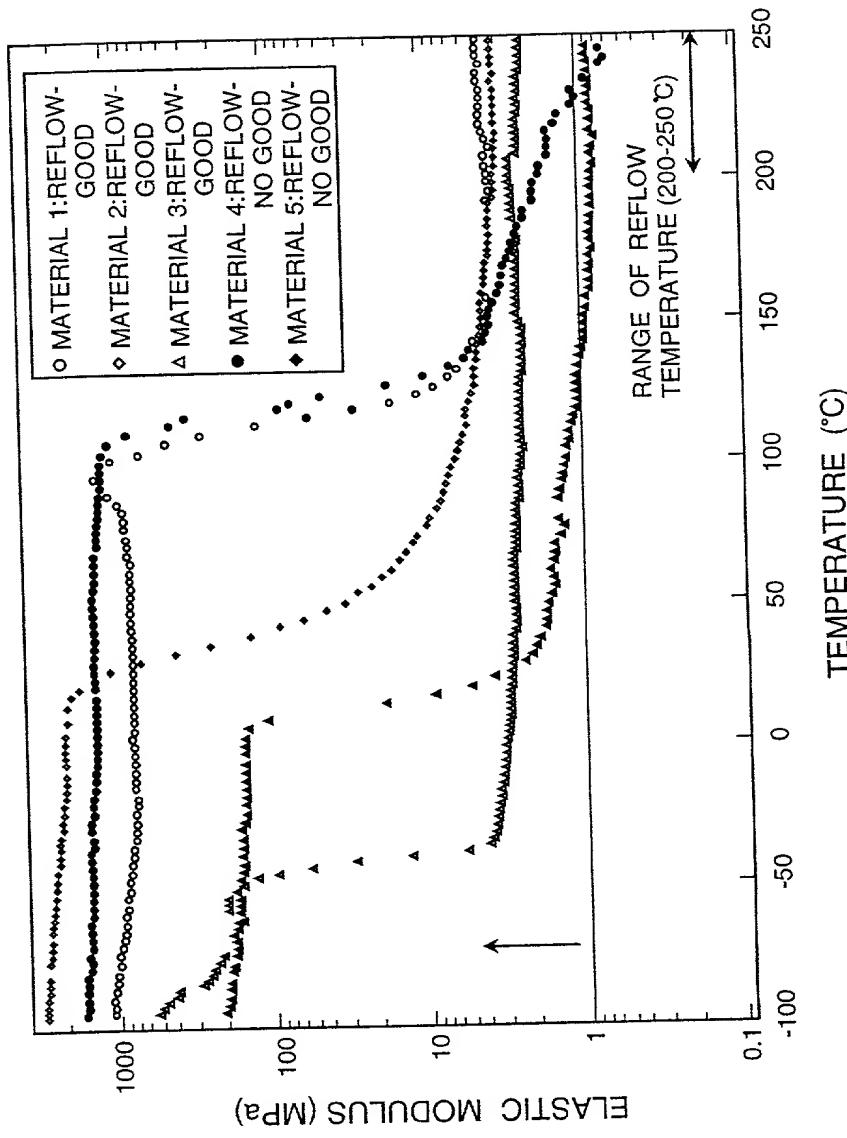


FIG.2

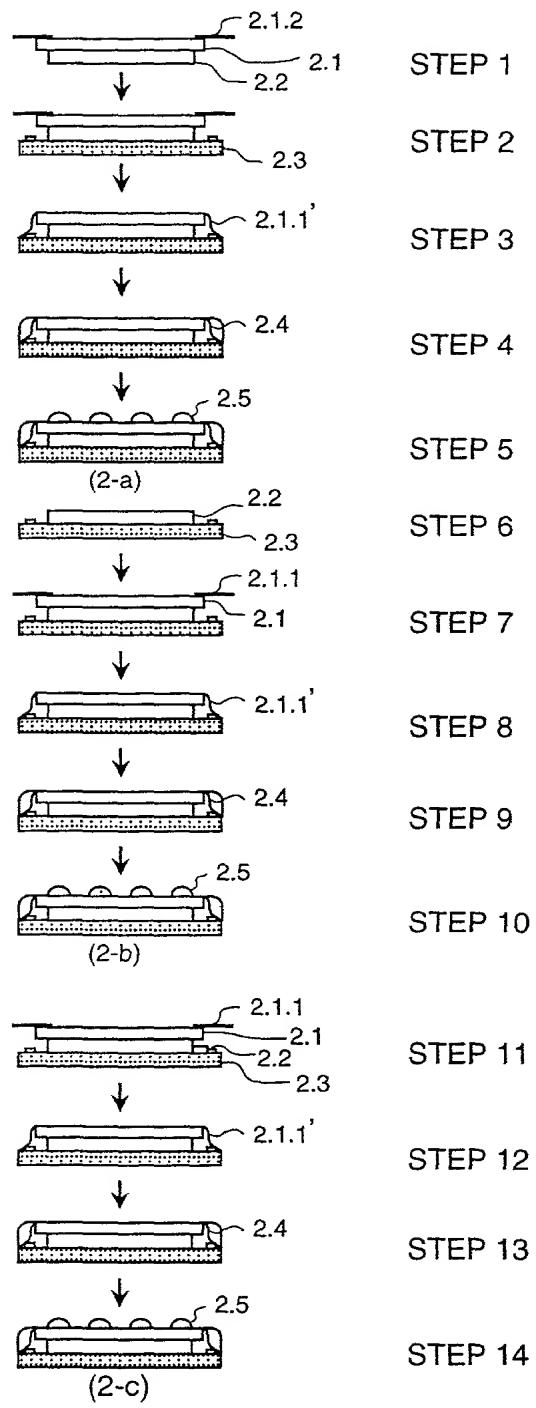


FIG.3

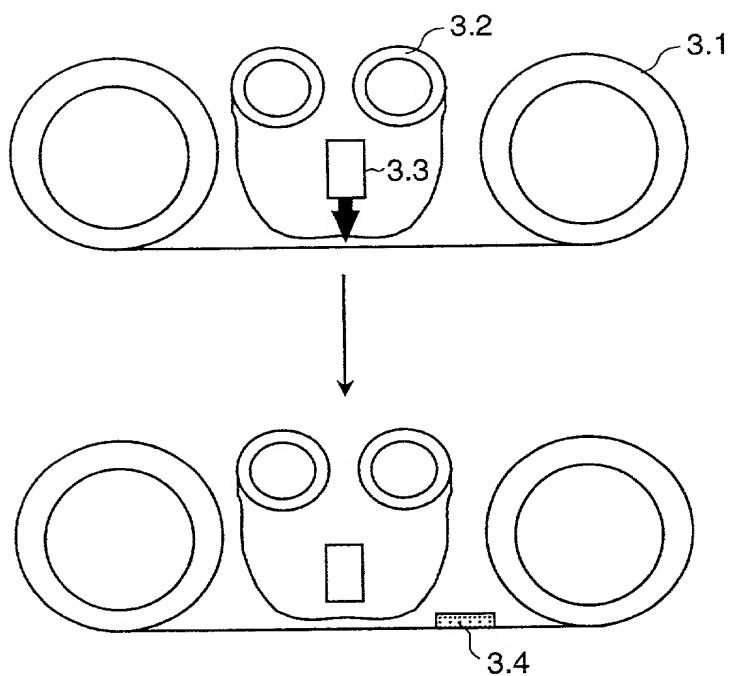


FIG.4

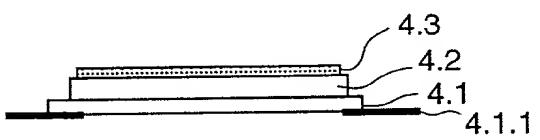


FIG.5

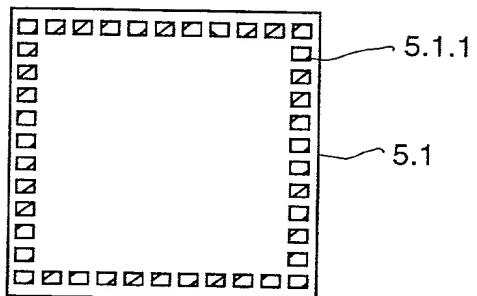
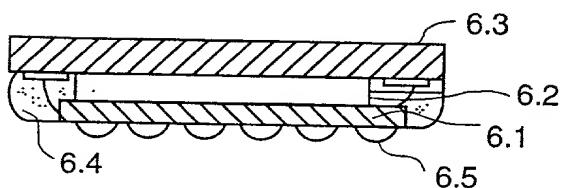
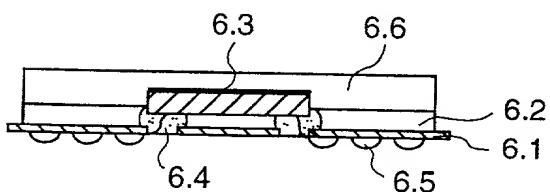


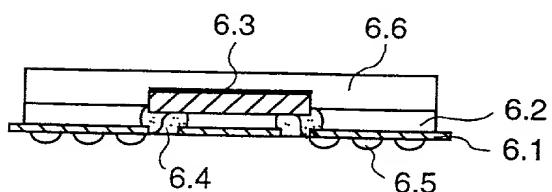
FIG.6



(6-1) Fan In TYPE



(6-2) Fan Out TYPE



(6-3) Fan In/Out TYPE

FIG.7

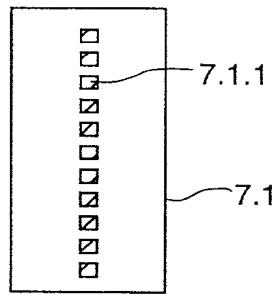
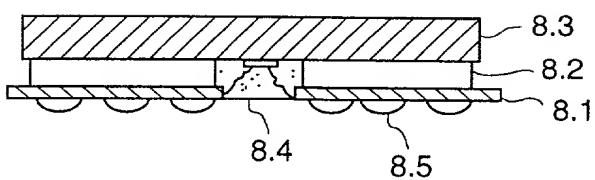


FIG.8



DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name, I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

CIRCUIT TAPE HAVING ADHESIVE FILM, SEMICONDUCTOR DEVICE, AND A METHOD FOR MANUFACTURING THE SAME

the specification of which (check one) is attached hereto.

was filed on _____
as Application Serial No. _____
and was amended on _____
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)

Priority Claimed

8-136159 (Number)	Japan (Country)	30/05/1996 (Day/Month/Year Filed)	<input checked="" type="checkbox"/> Yes	<input type="checkbox"/> No
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	<input type="checkbox"/> Yes	<input type="checkbox"/> No
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	<input type="checkbox"/> Yes	<input type="checkbox"/> No
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	<input type="checkbox"/> Yes	<input type="checkbox"/> No
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	<input type="checkbox"/> Yes	<input type="checkbox"/> No
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	<input type="checkbox"/> Yes	<input type="checkbox"/> No

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Apphcation Serial No.)	(Filing Date)	(Status: patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status: patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status: patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status: patented, pending, abandoned)

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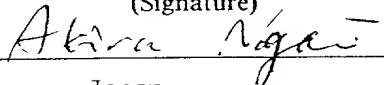
I hereby appoint as principal attorneys; Donald R. Antonelli, Reg. No. 20,296; David T. Terry, Reg. No. 20,178; Melvin Kraus, Reg. No. 22,466; Stanley A. Wal, Reg. No. 26,432; William I. Solomon, Reg. No. 28,565; Gregory E. Montone, Reg. No. 28,141; Ronald J. Shore, Reg. No. 28,577; Donald E. Stout, Reg. No. 26,422; Alan E. Schiavelli, Reg. No. 32,087; James N. Dresser, Reg. No. 22,973 and Carl I. Brundidge, Reg. No. 29,621 to prosecute and transact all business connected with this application and any related United States application and international applications. Please direct all communications to the following address:

Antonelli, Terry, Stout & Kraus
Suite 1800
1300 North Seventeenth Street
Arlington, Virginia 22209
Telephone: (703) 312-6600
Fax: (703) 312-6666

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

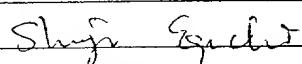
(Full Name)

(Signature)

Date April 24, 1997 Inventor Akira Nagai 

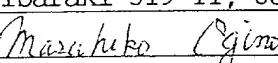
Residence Same as Post Office Address Citizenship Japan

Post Office Address A406, 14, Higashitaga-cho 3-chome, Hitachi-shi, Ibaraki 316, Japan

Date April 24, 1997 Inventor Shuji Eguchi 

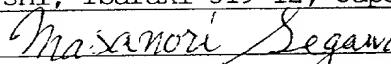
Residence Same as Post Office Address Citizenship Japan

Post Office Address 1711-30, Shirakata, Toukai-mura, Naka-gun, Ibaraki 319-11, Japan

Date April 24, 1997 Inventor Masahiko Ogino 

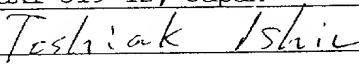
Residence Same as Post Office Address Citizenship Japan

Post Office Address 19-1-402, Ishinazaka-cho 1-chome, Hitachi-shi, Ibaraki 319-12, Japan

Date April 24, 1997 Inventor Masanori Segawa 

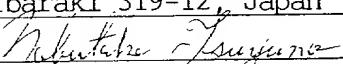
Residence Same as Post Office Address Citizenship Japan

Post Office Address 33-10, Kuji-cho 3-chome, Hitachi-shi, Ibaraki 319-12, Japan

Date April 24, 1997 Inventor Toshiaki Ishii 

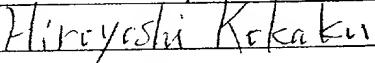
Residence Same as Post Office Address Citizenship Japan

Post Office Address 7-6-104, Oomika-cho 6-chome, Hitachi-shi, Ibaraki 319-12, Japan

Date April 24, 1997 Inventor Nobutake Tsuyuno 

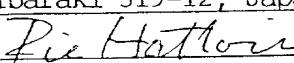
Residence Same as Post Office Address Citizenship Japan

Post Office Address Yuhou-ryo B506, 20-3, Ayukawa-cho 6-chome, Hitachi-shi, Ibaraki 316, Japan

Date April 24, 1997 Inventor Hiroyoshi Kokaku 

Residence Same as Post Office Address Citizenship Japan

Post Office Address 24-9, Ishinazaka-cho 1-chome, Hitachi-shi, Ibaraki 319-12, Japan

Date April 24, 1997 Inventor Rie Hattori 

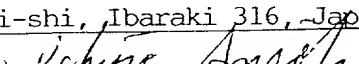
Residence Same as Post Office Address Citizenship Japan

Post Office Address 3466-2, Mawatari, Hitachinaka-shi, Ibaraki 312, Japan

Date April 24, 1997 Inventor Makoto Morishima 

Residence Same as Post Office Address Citizenship Japan

Post Office Address 20-1, Higashikanesawa-cho 5-chome, Hitachi-shi, Ibaraki 316, Japan

Date April 24, 1997 Inventor Ichiro Anjoh 

Residence Same as Post Office Address Citizenship Japan

Post Office Address 5-5, Nukuiminami-cho 4-chome, Koganei-shi, Tokyo 184, Japan

(Full Name)

(Signature)

Date April 24, 1997 Inventor Kunihiro Tsubosaki Kunihiro Tsubosaki

Residence Same as Post Office Address Citizenship Japan

Post Office Address 29-22, Higashihirayama 2-chome, Hino-shi, Tokyo 191, Japan

Date April 24, 1997 Inventor Chuichi Miyazaki Chuichi Miyazaki

Residence Same as Post Office Address Citizenship Japan

Post Office Address 7-3-302, Mihori-cho 2-chome, Akishima-shi, Tokyo 196, Japan

Date April 24, 1997 Inventor Makoto Kitano Makoto Kitano

Residence Same as Post Office Address Citizenship Japan

Post Office Address 1057-8, Shiratori-machi, Tsuchiura-shi, Ibaraki 300, Japan

Date April 24, 1997 Inventor Mamoru Mita Mamoru Mita

Residence Same as Post Office Address Citizenship Japan

Post Office Address 16-14, Tajiri-cho 3-chome, Hitachi-shi, Ibaraki 319-14, Japan

Date April 24, 1997 Inventor Norio Okabe Norio Okabe

Residence Same as Post Office Address Citizenship Japan

Post Office Address 4-9, Aita-cho 2-chome, Hitachi-shi, Ibaraki 319-14, Japan

Date _____ Inventor _____

Residence _____ Citizenship _____

Post Office Address _____

Date _____ Inventor _____

Residence _____ Citizenship _____

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Date _____ Inventor _____

Residence _____ Citizenship _____

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